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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/808,612	03/14/2001	Thomas J. Pennello	MWI.003A	4549

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GAZDZINSKI & ASSOCIATES
11440 WEST BERNARDO COURT, SUITE 375
SAN DIEGO, CA 92127

EXAMINER	
FERRIS III, FRED O	
ART UNIT	**PAPER NUMBER**
2128	

DATE MAILED: 02/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/808,612	PENNELLO ET AL.	
	Examiner	Art Unit	
	Fred Ferris	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *33-34* is/are allowed.

6)☒ Claim(s) *1-32 and 35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 5 October 2005 has been entered. Claims 1-35 have been presented for examination based on applicant's amendment filed on 30 November 2005. Claims 1-32 and 35 remain rejected by the examiner. Claims 33-34 have been allowed over the prior art of record.

Response to Arguments

2. Applicant's arguments filed 30 November 2005 have been fully considered.

Regarding applicant's response 102(e) rejections: The examiner withdraws the 102(e) rejection in view of applicants amendment to the claims and arguments submitted 30 November 2005.

Regarding applicant's response 103(a) rejections: The examiner withdraws the previous 103(a) rejection in view of applicant's amendment to the claims. Hence, applicant's arguments relative to the previous rejections are now moot. However, new prior art rejections have now been applied responsive to the amended claims. (See below)

Claim Interpretation

3. Applicants are disclosing and claiming a method and apparatus for debugging distributed programs by identifying and initializing processes, executing a thread to control processes, and cycling between processes to monitor status. As currently written, the independent claims appear to be broadly drawn to subject matter that is commonly known in the art as ***debugging of concurrent processes****. (See: "Debugging of Concurrent Processes", S. Grabner et al, IEEE 1066-6192/95, IEEE 1995, for example) Accordingly, the examiner has interpreted the claimed limitations relating to debugging of distributed programs as equivalent to techniques used in debugging of concurrent processes and has applied art rejections accordingly. (See: 102/103 rejections below)*

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1, 14, 19-24, and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,282,701 issued to Wygodny et al in view of U.S. Patent 6,117,181 issued to Dearth et al.

Independent claims 1, 19 and 22, for example, are drawn to:
Method for debugging distributed programs by:
Identifying processes
Initializing processes
Executing single thread of control among processes
Continuously switching between processes (without determining debug event) to obtain related status

Regarding independent claims 1, 14, 19-24, and 31: Wygodny discloses debugging distributed programs over multiple processors, initializing processors, executing a control thread, switching between processes and obtaining status information. (Abstract, Background, CL2-L51-CL3-L43, Figs. 1A-2).

Wygodny renders obvious the elements of the aforementioned independent claims as follows:

- Method for debugging distributed programs: Wygodny discloses debugging processes in a distributed (varied) processor (i.e. heterogeneous) environment (Abstract, CL3-L13-26).

- Identifying processes: Wygodny discloses (selectively) identifying among hierarchical processes (CL8-L64, Figs. 6-8) during the debugging process.

- Initializing processes: Wygodny discloses initiating processes with initial parameters such as process information, code, variables, and indicators, (i.e. initializing the processes) and starting/restarting the debugging of processes (CL24-L50-67).

- *Continuously switching between processes to obtain related status: Wygodny teaches continuously polling between processes in order to monitor the "status" of each pending debug process (CL8-L52-CL9-L57). Wygodny polls to monitor the status of process information, code, variables, and indicators (Fig. 3A, Tab. 1) in the debugging process and outputting the information (Figs. 5-14) regardless of event.*

Wygodny does not explicitly disclose that the control be via a single thread.

Dearth discloses executing a thread (single) as part of the control process among processes (CL6-L33-61).

It would have been obvious to one having ordinary skill in the art at the time the claimed invention was made to modify the teachings of Wygodny relating to debugging distributed programs over multiple processors, with the teachings of Dearth relating to executing a thread (single) as part of the control process among processes, to realize the elements of the claimed invention. An obvious motivation exists since the Wygodny et al reference teaches multiple threading in debugging process while Dearth teaches that a single thread can control debug processes allowing for more efficient debugging with less processor overhead (See: Wygodny/Dearth Summary). Further, the level of skill required by an artisan to realize the claimed limitations of the present invention is clearly established by both references. (See: Wygodny/Dearth, Abstract) Accordingly, a

skilled artisan tasked with realizing a method for debugging a plurality of processes in a multi-processing environment, and having access to the teachings of Wygodny and Dearth, would have knowingly modified the teachings of Wygodny with the teachings of Dearth to realize the claimed elements of the present invention while gaining the advantage of more efficient debugging with less processor overhead.

5. Claims 2-13, and 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,282,701 issued to Wygodny et al in view of U.S. Patent 6,117,181 issued to Dearth et al in further view of U.S. Patent 6,230,307issued to Davis et al.

Regarding dependent claims 2-4: Davis teaches the elements of the limitations of independent claims 2-4 as follows:

- *simulation process: Davis discloses the simulation (emulation) for both a* ***hardware and software*** *realization of circuit (object) elements (Abstract, CL1-L25-55, CL4-L 51-58, CL24-L16-18, Figs. 1, 6 and 9).*
- *hardware process: As noted above, Davis discloses the simulation (emulation) for both a* ***hardware and software*** *realization of circuit (object) elements (Abstract, CL1-L25-55, CL4-L 51-58, CL24-L16-18, Figs. 1, 6 and 9).*
- *analyzing status for errors: Davis discloses determining the status (i.e. analyzing status) of various object elements and detecting and responding to the occurrence of errors. (CL12-L23-33, Fig. 17, CL42-L49) (Merks discloses monitoring status as noted above)*

- *defining object classes: Davis discloses defining hardware object classes for emulated (simulated) circuit element (CL9-L54-67, CL10-L1-39, Figs. 11, 12)*
- *defining object **subclasses** for hardware and simulation processes: Davis further discloses defining subclasses for the hardware simulation (emulation) processes (CL11-L43-56, CL9-L5-24, Fig. 15)*

Regarding dependent claims 5-13, 15-18: Davis teaches the elements of the limitations of independent claims 5-14 as follows:

- *first instance variable controlling processes: Davis discloses using variables in the thread based scheduling and controlling of processes from an initial (first) state (CL3-L32-37, CL7-L56,CL9-L25-53, CL12-L15-23, Fig. 17).*
- *dynamically changing polling time of process based on status: Davis discloses the use of various primitives for setting parameters relating to dynamically scheduling/dispatching tasks which can effect (change) the scheduling (polling) time for process execution and management (CL12-L15-37). (Merks also discloses a variable rate polling time as noted above)*
- *interface for defining/accessing library of hardware processes: Davis discloses defining, accessing, and interfacing to a library of dynamically re-configurable hardware processes. (CL5-L52-64, CL6-L14-33, CL8-L39-64, Figs. 3, 4, 9)*
- *library includes extension instructions: Extension instructions are reserved processor instruction set by the processor manufacturer, and hence would have been an obvious feature to include in the library of hardware processes. (See applicant's specification page 7, line 5-12)*

- *initializing hardware simulator processes: Davis discloses beginning the thread controlled hardware simulation (emulation) process from a known initial (i.e. initialized) state. (CL9-L20-25, Fig 10)*
- *dynamically loadable library: Davis discloses a dynamically loadable and re-usable library (CL8-L54 to CL9-L5).*

It would have been obvious to one having ordinary skill in the art at the time the claimed invention was made to further modify the teachings of Wygodny and Dearth as noted above with the teachings of Davis relating to both hardware and software realization of circuit (object) elements, to realize the claimed invention. An obvious motivation exists since Wygodny, Dearth, and Davis all teach debugging of multiple processes. (See: Wygodny/Dearth/Davis Summary) Davis teaches that this can be extended to hardware and software debugging. Further, the level of skill required by an artisan to realize the claimed limitations of the present invention is clearly established by both references. (See: Wygodny/Dearth/Davisz, Abstract) Accordingly, a skilled artisan tasked with realizing a method for debugging a plurality of processes in a multi-processing environment that includes hardware and software, and having access to the teachings of Wygodny, Dearth, and Davis, would have knowingly further modified the teachings of Wygodny and Dearth with the teaching of Davis to realize the claimed elements of the present invention while gaining the advantage of more efficient debugging with less processor overhead in a hardware/software debugger.

Regarding claims 25, 27, 28, and 30: These claims include limitations relating to the determination of status information by periodically switching (i.e. polling) to determine status. These claims are therefore rendered obvious using the same reasoning as recited above. Namely, that the process of "polling" is very well known and commonly practiced in the art a means of "periodically determining the statues of a device or process" (Microsoft Computer Dictionary, 3rd Edition, 1997). Hence, a "polling" process would have necessarily been incorporated by a skilled artisan as a means of "determining whether an event of interest has occurred" between processes to obtain status information and if a debug event has occurred. Therefore, such features would have knowingly been incorporated by a skilled artisan using the same reasoning as set forth above.

Regarding claims 26, 29: These claims merely include additional limitations relating to extended processors. The examiner has asserted that the claimed "extended digital processors" are simply defined by applicants specification be processors capable of performing "extended operations". (Specification page 7, line 1-5). The examiner has submitted that it is well established that processors included extended instruction operations. (See: "Introduction to Computer Architecture", Stone, 1980, defining a typical example of such an extension instruction) The examiner therefore submits that the claimed "extended operations" would have knowingly been incorporated by a skilled artisan using the same reasoning as set forth above.

6. Claims 31, 32, and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,282,701 issued to Wygodny et al in view of U.S. Patent 6,117,181 issued to Dearth et al in further view of U.S. Patent 5,101,491 issued to Katzeff.

Regarding claims 31, 32, 35: The combination of Wygodny and Dearth renders obvious the limitations relating to debugging distributed programs over multiple processors and simulation of hardware processes of library based circuit elements and previously cited above.

Wygodny and Dearth further do not explicitly disclose the elements relating to language independent debugging.

Katzeff teaches a language independent method (CL1-L55 to CL2-L11, Summary of Invention) of debugging process entities inclusive of a simulation of a hardware process (Figs. 1-3, 8, 9).

It would have been obvious to one having ordinary skill in the art at the time the claimed invention was made to further modify the teachings of Wygodny and Dearth as noted above with the teachings of Katzeff relating to language independent debugging, to realize the claimed invention. An obvious motivation exists since Wygodny, Dearth, and Krantz all teach the use of threads in multiple processes to improve the debugging process. (See: Wygodny/Dearth Summary) Krantz teaches that this can be extended to language independent debugging. Further, the level of skill required by an artisan to realize the claimed limitations of the present invention is clearly established by both references. (See: Wygodny/Dearth/Krantz, Abstract) Accordingly, a skilled artisan

tasked with realizing a method for debugging a plurality of processes in a multi-processing environment that includes language independency, and having access to the teachings of Wygodny, Dearth, and Krantz, would have knowingly further modified the teachings of Wygodny and Dearth with the teaching of Krantz to realize the claimed elements of the present invention while gaining the advantage of more efficient debugging with less processor overhead in a language independent debugger.

Allowable Subject Matter

7. Claims 33 and 34 are allowed over the prior art of record. In this case, the prior art does not explicitly disclose the specific sequence of steps relating to advancing tru instruction cycle based on simulation type, hardware type, and status checking, where processes gather status information of heterogeneous processors based on a dynamic per-process time interval as now required by independent claim 33.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure, careful consideration should be given prior to applicant's response to this Office Action.

U.S. Patent 6,718,294 issued to Bortfeld teaches debugging concurrent processes in a multi-simulator environment.

"Debugging of Concurrent Processes", S. Grabner et al, IEEE 1066-6192/95, IEEE 1995, teaches debugging concurrent processes in a multi-simulator environment.

"A Concurrent Program Debugging Environment using Real-time Replay", E.H. Piak et al, IEEE 0-8186-8227-2/97, IEEE 1997, teaches debugging concurrent processes in a multi-simulator environment.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fred Ferris whose telephone number is 571-272-3778 and whose normal working hours are 8:30am to 5:00pm Monday to Friday. Any inquiry of a general nature relating to the status of this application should be directed to the group receptionist whose telephone number is 571-272-3700. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean Homere can be reached at 571-272-3780. The Official Fax Number is: (703) 872-9306

Fred Ferris, Primary Examiner
Simulation and Emulation, Art Unit 2128
U.S. Patent and Trademark Office
Randolph Building, Room 5D19
401 Dulany Street
Alexandria, VA 22313
Phone: (571-272-3778)
Fred.Ferris@uspto.gov
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